IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Cancelled).

Claim 2 (Currently Amended): A multiprocessor system comprising:

a plurality of processors;

~~at least one~~ a plurality of debug executing ~~unit~~ units for respectively executing the debugging of each of said plurality of processors;

~~at least one controller~~ a plurality of controllers for respectively controlling each of said debug executing ~~unit~~ units;

a set of terminals to be connected to an external debugging device; and

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processors to be debugged, wherein

said plurality of processors comprise first and second processors,

said plurality of debug executing ~~unit~~ units comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor,

said plurality of controllers ~~controller~~ comprises a first controller connected to said first debug executing unit and a second controller connected to said second debug executing unit,

said selecting circuit is connected between said first and second controllers and said set of terminals, and

said selecting circuit inputs, to one or both of said first and second controllers, a debugging signal that is provided commonly from said debugging device through said set of terminals.

Claim 3 (Previously Presented): A multiprocessor system comprising:

a plurality of processors;

at least one debug executing unit for executing the debugging of said plurality of processors;

at least one controller for controlling said debug executing unit;

a set of terminals to be connected to an external debugging device; and

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processors to be debugged, wherein

said plurality of processors comprise first and second processors,

said debug executing unit comprises a first debug executing unit connected to said first processor and a second debug executing unit connected to said second processor,

said selecting circuit is connected between said first and second debug executing units and said controller,

said controller is connected to said set of terminals, and

said selecting circuit inputs, to one or both of said first and second debug executing units, a debugging signal outputted from said controller.

Claim 4 (Previously Presented): A multiprocessor system comprising:

a plurality of processors;

at least one debug executing unit for executing the debugging of said plurality of processors;

at least one controller for controlling said debug executing unit;

a set of terminals to be connected to an external debugging device; and

a selecting circuit for selecting, from among said plurality of processors, part or all of said plurality of processors to be debugged, wherein

said plurality of processors comprise first and second processors,

said selecting circuit is connected between said first and second processors and said debug executing unit,

said debug executing unit is connected to said controller,

said controller is connected to said set of terminals, and

said selecting circuit inputs, to one or both of said first and second processors, a debugging signal outputted from said debug executing unit.

Claim 5 (Previously Presented): The multiprocessor system according to claim 2, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis of setting of a given register.

Claim 6 (Currently Amended): The multiprocessor system according to claim 2, wherein said selecting circuit selects said part or all of said plurality of processors to be debugged, on the basis of a select signal ~~inputted~~ input to a given terminal from an external source ~~outside~~.

Claims 7-10 (Cancelled).